Solution-Processed Complementary Resistive Switching Arrays for Associative Memory

Jeremy Smith, *Member, IEEE*, Seungjun Chung, Jaewon Jang, *Member, IEEE*, Carlos Biaou, *Member, IEEE*, and Vivek Subramanian, *Member, IEEE*

***Abstract*— Complementary resistive switches (CRS) based on back-to-back nanofilamentary resistive RAM devices have been fabricated by an all-solution-processed method, employing inkjet-printed Ag and Au contacts and a spin-coated sol–gel zirconium oxide dielectric layer. The devices demonstrate electrical switching behavior below 3 V, stable on-state windows, reasonable cycle lifetimes, and can be implemented in 2×2 memory arrays with no crosstalk during addressing. For reliable operation and high yields of the CRS devices, printing and annealing processes were carefully optimized to eliminate the coffee-ring effect on the bottom electrode, and produce a pin-hole free dielectric. The arrays are fully pulse programmable and are able to retain their state for $>10^4$ s. Additionally, the arrays can be operated as associative or content addressable, memory for pattern matching applications, which is demonstrated through a basic hamming distance mapping measurement for different stored data states.**

***Index Terms*— Associative memory, inkjet printing, resistive RAM (RRAM), thin-film devices, zirconium oxide.**

I. Introduction

SOLUTION processing of functional materials for next-generation electronics has become a significant field in the last two decades. A diverse range of materials has been studied for this application, ranging from organic molecules, to oxides, to nanomaterials. Such materials can exhibit properties that span the spectrum of dielectric, semiconducting, and metallic behaviors, and can be deposited from solution using a variety of chemistries and techniques such as printing, spray coating, dip coating, or spin coating. Novel applications that employ solution-processed devices are often focused on low cost, large area, flexible, transparent, and/or printable electronics, and include thin-film transistors, solar cells, light-emitting diodes, sensors, and memory. Several examples of solution-processed memory have been previously demonstrated based on resistive switching [1]–[8] or the use of transistor-like devices [9]–[12], and flexible memory has been fabricated by thin-film transfer methods [13], [14]. However, integration into arrays and device scaling are still significant challenges. Processing and materials complexities, printing resolution, and device-to-device uniformity are some of the key areas that need to be addressed. Additionally, suitable applications for this technology must be considered; although unlikely to replace traditional high-density, high-performance memory, there is the potential for innovative memory integration into large-area electronics, biologically inspired electronics, wearable electronics, or low-cost electronics for the internet of things (IoT).

The field of resistive switching for nonvolatile memory applications has been widely researched due to its potential for low power consumption, high density of devices, simple architecture, and fast switching speed. Resistive RAM (RRAM) commonly employs transition metal oxides such as Ta_2O_5, NiO, TiO_2, HfO_2, and ZrO_2 as the dielectric material in a metal–insulator–metal (MIM) geometry [15]. The mechanism of operation typically involves the reversible formation of nanoscale conductive filaments within the oxide that can bridge between metallic contacts, thus giving rise to a low-resistance state (LRS) and high-resistance state (HRS). These filaments can either be the result of metal bridges, or conductive pathways formed due to defect creation in the oxide. To utilize such devices in an addressable memory array, a selector, or rectifying behavior of the RRAM itself, is required to prevent current sneak paths between memory locations. Recently, complementary resistive switching (CRS) using two back-to-back RRAM elements has been demonstrated as an alternative to the separate selector approach [16]. This type of structure can simplify the memory architecture by reducing the number of unique materials that have to be deposited, which is especially desirable in the case of solution-processed electronics. However, more importantly, it also results in extremely interesting nonlinear switching behavior that can be utilized for nontraditional computing such as mimicking synaptic [17], [18], and multilevel

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J. Smith, C. Biaou, and V. Subramanian are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA (e-mail: j.smith.03@cantab.net; viveks@eecs.berkeley.edu).

S. Chung was with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA. He is now with the Department of Physics and Astronomy, Seoul National University, Seoul 08826, South Korea.

J. Jang was with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA. He is now with the School of Electronics Engineering, Kyungpook National University, Daegu 41566, South Korea.

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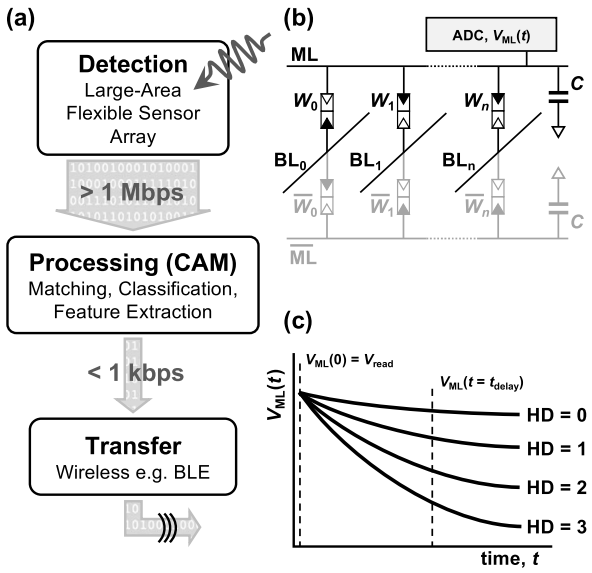

Fig. 1. (a) Schematic data flow through a large-area sensor device with a processing layer that includes CAM and wireless transfer of data off-device. (b) Schematic of a CRS associative memory architecture. A single ML and its complement are shown with stored bits W_n, and corresponding BLs. (c) ML voltage $V_{ML}(t)$ is measured as a function of time and typical outputs are displayed for different values of the HD between stored data and test data applied to the BLs.

behavior [19], [20], stateful logic [21], or in the case of this paper, associative memory. This last application is particularly interesting for large-area electronics since, in conjunction with proposed applications of such systems in sensors [22]–[24], associated memories may enable robust pattern matching for sensor output identification.

II. Associative Memory for Printed Electronics

There is currently a drive to develop improved associative memory architectures that are content, rather than location, addressable for efficient data matching and classification applications [25], [26]. However, typically content addressable memory (CAM) requires more area and devices per memory cell, and consumes more power than an equivalent location addressable memory. Therefore, it has been suggested that CRS arrays can be used to perform Hamming distance (HD) mapping between stored and test data, and thus display CAM functionality [27], [28]. The readout in these cases can either be performed capacitively or resistively. In the latter, by measuring match line (ML) discharge caused by CRS devices switching to their low resistance ON-state as a result of bit level mismatches, it is possible to read a voltage that is proportional to the number of bits that are switched (Fig. 1). This technique has the potential to yield high-density, low-power CAM circuits with an output directly related to the HD.

Solution-processed CRS arrays are attractive, not only for their ability to be used as CAM, but also because of their relatively simple structure, the limited number of materials required, and their compatibility with other solution-processed electronics. Printable memory arrays have motivating applications in terms of integration into such systems to provide local data processing and storage. This technology could be useful for low-cost distributed sensor networks, and flexible, large-area sensor arrays. By performing pattern matching and feature extraction in proximity to a sensor array, there are significant energy efficiency savings associated with the reduced transfer of data off-chip for processing (Fig. 1). Although on-chip processing power would also have to be considered, wireless transmission power would be the limiting factor provided that CAM read cycles are short [26]. For example, a modest 100×100 sensor array operating at 10 Hz (0.1 Mbps) would require $\sim$4 mW of power to transmit these data using current Bluetooth LE technology (calculation given in the Appendix). This is already unfeasible for ultralow-power systems and for larger arrays would rapidly become impossible for any battery powered device. On-chip data classification and pattern matching could drastically reduce this power consumption by lowering data rates by several orders of magnitude.

While the low carrier mobility of solution-processed semiconductors limits their ability to compete with silicon logic for data processing, there is in theory no such restriction for resistive switching performance, provided that there are no limitations from the circuit itself. For example, the switching times for a wide range of oxide RRAM systems fall into the 1–100 ns range [15]. Therefore, the use of solution-processed resistive switching devices, such as those based on CRS, and an understanding of their structural and electronic properties are critical for enabling novel functionality that can allow basic memory and data processing in fully printable electronics.

In this paper, we focus on the Ag/ZrO_2/Au system, which operates through the formation of Ag metallic bridges and has a relatively low forming voltage and fast switching speed due to the high diffusivity of Ag^+ in ZrO_2 [29]–[31]. Both Ag and Au metallic nanoparticle inks and metal oxide sol–gel inks for the dielectric are individually relatively well understood. Therefore, the fabrication of fully solution-processed MIM devices is straightforward in comparison to some other potential RRAM systems. This paper, however, represents the first demonstration of printed CRS devices and their application in arrays with realistic memory addressing. The use of CRS devices as CAM is a comparatively unexplored area in itself; therefore, the fact that we are able to implement this with printed electronics is very significant and then opens up novel ways to perform computation with large-area electronics.

III. Device Fabrication

All CRS devices were fabricated on Corning 1737 glass substrates. A lateral back-to-back architecture was employed with two array types being fabricated: fully printed contacts and hybrid bottom contacts. Photolithographically patterned Cr/Au (5 nm/45 nm) interconnects were patterned by lift-off for the hybrid contacts, while inkjet-printed Au and Ag were deposited using a Ceradrop X-serie materials printer. The Au nanoparticle ink was obtained from Harima Chemicals (NPG-J) and Ag ink from Advanced Nano Products (DGP 40LT-15C), and both were loaded into 1- or 10-pL Dimatix inkjet cartridges depending on the type of device. Jetting conditions for the two inks are listed in Table I. Substrates were solvent cleaned and treated with 1 min of oxygen plasma (50 W-RF, 100 mTorr) before Au printing.

TABLE I
INKJET-PRINTING PARAMETERS

Parameter	Au ink (Harima NPG-J)	Ag ink (Advanced Nano)
Platten temperature (°C)	30	32
Nozzle temperature (°C)	35	35
Max waveform voltage (V)	25	23
Jetting frequencies (Hz)	150 (drops) 1000 (lines)	150 (drops) 2000 (lines)

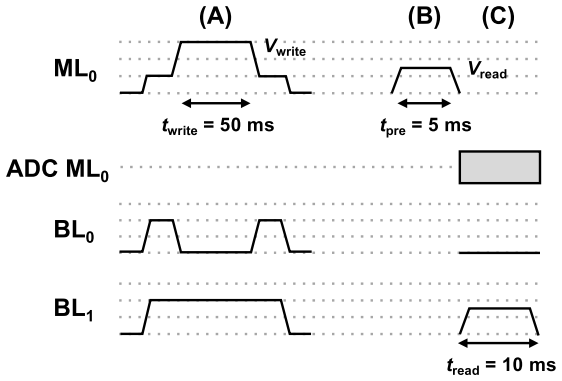

Fig. 2. (A) Pulse train for memory testing demonstrating an example write event. (B) ML precharge. (C) Content-addressable read. First, a 0-state is written to the location (ML_0, BL_0) using a 1/3–2/3 V_{write} scheme. Once all states are programmed, ML_0 is precharged to the read voltage V_{read}. Last, the content addressable read on ML_0 is preformed using the data pattern (BL_0, BL_1) = (0, 1) and the A/D converter on ML_0.

Inkjet-printed lines and pads were deposited with drop spacings of 30–40 μm depending on the required thickness. The films were subsequently ramped to 245 °C for 30 min to sinter the Au nanoparticles. Multiple ZrO_2 layers were deposited by spin coating a sol–gel precursor, zirconium acetylacetonate (0.1 M in 10-mL EtOH with 400-μ L monoethanolamine), at 3000 rpm for 30 s. Before spinning, substrates were cleaned for 2 min in an air plasma (50 W-RF, 100 mTorr). Films were dried at 290 °C for 5 min between each layer. After spinning all layers, the films were annealed for 1 h at 500 °C in dry air. The top surface was then treated with 2-min UV-ozone exposure before Ag ink printing. Finally, Ag nanoparticle sintering was carried out at 150 °C for 30 min.

IV. MEMORY TESTING

Pulsed and I–V sweep measurements on the memory arrays were carried out in ambient. Endurance and retention tests were performed with 100-ms read/write pulses using a multipulse programming scheme with a typical write voltage of ±3 V and a read voltage of 1–1.6 V. HD measurements were made using a custom program/read setup. ML and bit lines (BLs) were addressed with analog multiplexers controlled by an Arduino Mega 2560 microcontroller. A 1/3–2/3 V_{write} scheme was used to program the array, and the ML voltage was measured as a function of time using the A/D converter (41 kHz, 10-b) on the microcontroller (Fig. 2). The ML capacitance was set to 1 μF to achieve suitable voltage decay times based on the LRS and HRS resistances.

V. RESULTS AND DISCUSSION

The CRS device structure is shown in Fig. 3 along with images of the fully printed contact and hybrid bottom

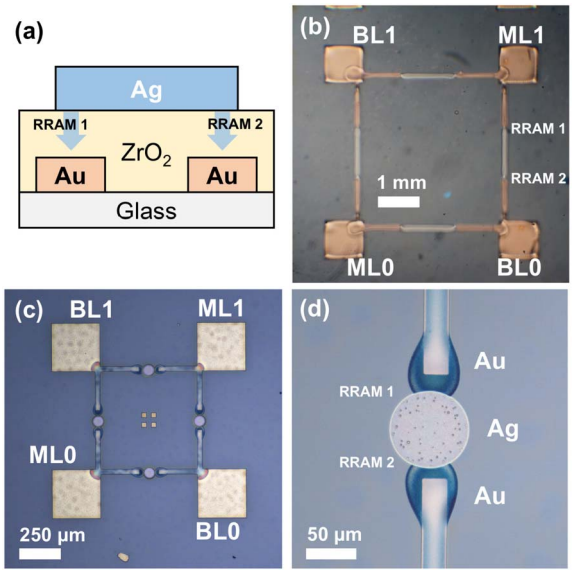

Fig. 3. (a) Diagram of a single lateral CRS device processed on glass with Au bottom contacts, a sol–gel ZrO_2 dielectric layer, and an Ag top contact. Arrows indicate diffusion of Ag^+ during forming in the two individual RRAM devices. Optical micrographs of 2 × 2 CRS arrays with (b) fully printed contact structure and (c) hybrid bottom contact structure. (d) Higher magnification view of a single CRS device in the hybrid bottom contact structure showing the printed, three-drop design.

contact arrays. The CRS devices are arranged in a 2 × 2 array with Au contacts for the MLs and BLs, and a top Ag electrode. The ZrO_2 consists of five spin-coated layers giving a total thickness of 65–70 nm on glass. The thickness of the ZrO_2 over the Au contact regions was found to be slightly lower but this did not adversely affect devices as long as the printed Au lines were kept below a thickness of ~60 nm. Above this resulted in a large number of electrically shorted devices. The Au printing was therefore optimized to have good conductivity, low thickness, and importantly, minimal coffee-ring effect, since the latter would produce line edges that could protrude through the ZrO_2. A hydrophilic glass surface, created by oxygen plasma treatment, prevented overwetting of the hydrophobic Au ink and resulted in a suitable line morphology. In the case of the fully printed contacts, the device overlap area was defined by printing an Ag line such that the end of the line coincides with the start of an Au line and vice versa. This generally gave active device areas in the range of 1000–5000 μm^2. Individual RRAM characteristics for these printed Ag/ZrO_2/Au systems, measured by contacting the Ag interconnect, are shown in Fig. 4(a) and (b). Devices had low leakage in their pristine state and adequate reliability and yield. The electrical yield of individual RRAMs during testing with a current compliance of 1 mA was generally >90%. Forming voltages were low and often equal to the SET voltage suggesting that Ag filaments grow very readily in the ZrO_2 layer, as expected for this system. During switching, SET and RESET voltages are well matched at around 1 V; however, two SET processes could typically be observed. Setting a current compliance of 100 μ A captures the initial SET at 1 V, whereas at 1 mA, the second SET can be observed at 1.5–2 V. This may be indicative of overgrowth of Ag filaments or partial conduction through the ZrO_2 by

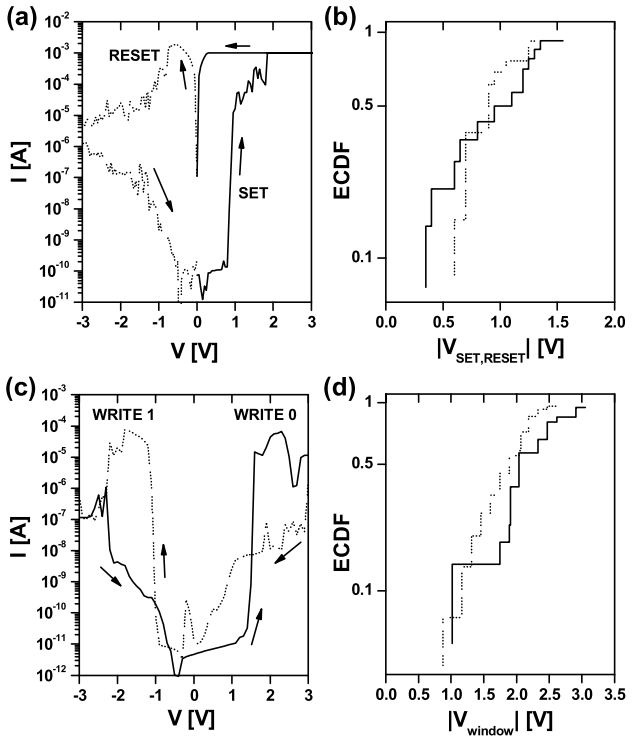

Fig. 4. (a) *I–V* characteristics of a single RRAM device showing bipolar switching behavior. Current compliance was set to 1 mA. (b) Experimental cumulative distribution (ECDF) of SET and RESET voltages for the individual RRAMs ($N = 13$). (c) *I–V* characteristics of a CRS device showing forward and reverse scans and therefore 0- and 1-states. (d) ECDF of the position of the center of the on-window V_{window} for both 0- and 1-states ($N = 20$).

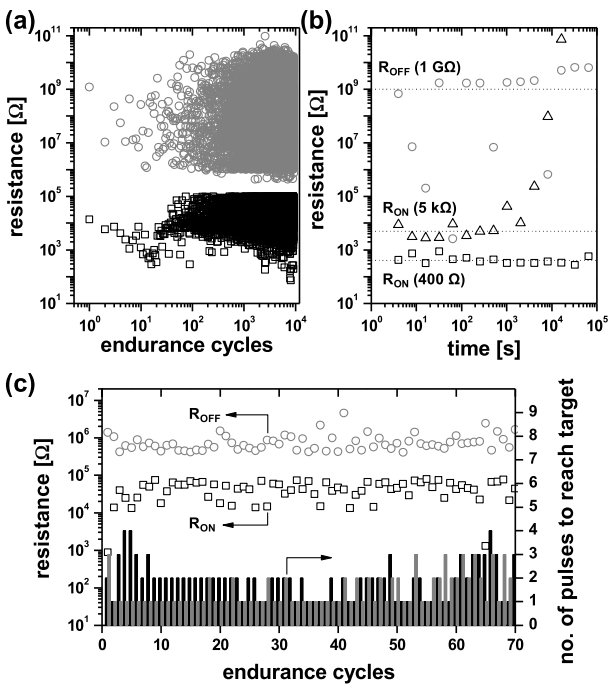

Fig. 5. (a) Cycle endurance behavior for a fully printed CRS device. (b) Retention time of the 0- and 1-states of the CRS device. In the case of the 0-state where a low resistance (R_{ON}) is measured when read, two different starting values of R_{ON} are shown (500 Ω and 8 kΩ). (c) First 70 endurance cycles of a printed hybrid bottom contact CRS device showing ON- and OFF-resistances and numbers of pulses required to reach the target resistance for each cycle. All cycle and retention tests were pulse programmed with read and write pulses of 100 ms.

defect pathways. However, when used in the CRS structure the current is limited by the second RRAM element, and so we can utilize the SET event at 1 V. A further requirement for achieving CRS behavior is that ideally $|V_{SET}| < 2|V_{RESET}|$, which, in this case, we fulfill.

In the fully printed contact devices, the overall array area is relatively large in order to facilitate ease of printing. Additionally, obtaining consistent device overlap area is extremely difficult due to the line printing approach. These effects tend to increase device-to-device variation, which is a problem for large arrays. Therefore, we would ideally like to be able to: 1) scale this process down to the limit of our inkjet-printing system to improve memory density and 2) realize devices with a small and consistent device area to help improve uniformity and reliability. To this end, we fabricated hybrid devices with printed CRS elements but evaporated interconnects, as shown in Fig. 3(c)and (d). A single ink drop is deposited for each Au electrode with an overlapping Ag drop to complete the CRS device. The drop position repeatability is approximately 2 μm, thus we can achieve an RRAM active area of 270 ± 20 μm^2 and an overall CRS area of 9200 ± 100 μm^2. This approach significantly improves on the fully printed structure by reducing the active area by a factor of at least four and reducing device-to-device variation caused by differences in device area. Note that such a system could also be achieved in a fully printed scheme by, for example, combing inkjet with gravure printing, the latter of which can deliver high resolution and excellent pattern fidelity [32].

The *I–V* characteristics of a typical back-to-back CRS device and the distribution of the positions of the ON-state windows are shown in Fig. 4(c)and (d). Devices follow the expected behavior for a CRS structure, with the two logic states defined by which of the two component RRAM elements is in an ON-state. Both fully printed and hybrid contact structures gave working CRS behavior, however, higher electrical yields and more consistent ON-state resistances were possible with the hybrid structure. As expected for a 1-V SET and RESET the ON-state window is predominantly between 1 and 2 V. These characteristics allow us to pulse program, erase, and read the devices with a write voltage of ~3 V and a read voltage of ~1.5 V. There is a clear resistance difference in the ON-window between the 0- and 1-states and low current within the OFF-window. For array programming, a 1/3–2/3 V_{write} scheme is required for CRS devices with large ON-state windows to prevent unintentional switching of nonaddressed elements [33]. Given the characteristics in Fig. 4, this method is effective for our system and allows us to program a 2×2 array.

Endurance and retention time for the CRS devices are shown in Fig. 5. Endurance of around 10^4 cycles was measured in the fully printed structures with failure typically occurring as a result of the loss of the OFF-window and one or both of the RRAM devices remaining in their ON-state leading to the CRS failing to its LRS. A multiple-pulse write scheme was used with target resistances for the LRS and HRS. For optimized arrays using 100-ms pulses, generally fewer than four pulses were required to reach the target resistance, which

is critical for their use in more complex addressing. For their use in CAM, a constant ON-state resistance is preferable since, along with the capacitance, this determines the decay time of the ML voltage. Therefore, another advantage of the hybrid contact devices can be seen in the range of R_{on} values during pulse programming being 10–70 kΩ compared to 500 Ω–100 kΩ for the fully printed contact structure. Retention times up to 10^5 s were observed for both 0- and 1-states, although the low resistance retention time has a dependence on the initial starting resistance at $t = 0$ s. For higher resistances, which generally correspond to narrower Ag filaments, a shorter retention time ($\sim 10^4$ s) was observed as the filaments redissolve into the ZrO_2. It should also be noted that there is some noise in the 1-state measurement due to the nature of the destructive read requiring the device to be reprogrammed for each time point. Since there is some spread in the number of program/erase pulses required, switching was not always guaranteed after the first pulse. Also, failure of the 1-state by both RRAM elements changing to their HRS is not detected; therefore, the 0-state measurement is a more useful measure of CRS retention.

The CAM functionality of the 2×2 arrays was tested by performing an HD measurement between 2-b data stored in the array and an external test sequence applied to the BLs. The truth table for the HD mapping is shown in Table II for a 2×2 array with both data and complementary data storage for the cases of $(W_0, W_1) = (1, 0)$ and $(W_0, W_1) = (0, 0)$. The mode of operation is that after precharging the ML to a voltage equal to the read voltage, the possible data combinations are applied to the BLs [(0, 0), (0, 1), (1, 0), or (1, 1)]. If these data result in a voltage drop across the CRS device, and the state of the device is such that it will switch state, then the ML will discharge as the CRS device enters its ON-window. It is therefore apparent why the complementary data are also required for complete matching since both of these conditions must be met, i.e., without the complementary data, HD is not equal to ML voltage decay in all cases and for full HD mapping we must use two MLs.

In a practical circuit, V_{ML} would be measured at a fixed delay time and a comparator circuit used to determine HD. In our case as a proof of concept, $V_{ML}(t)$ was measured and the results are displayed in Fig. 6. Four separate array measurements are shown for a read voltage of 1.6 V and write voltage of ±3 V. Note that these results are for a single ML, and therefore correspond to each of the possible stored data combinations in Table II. To obtain the full HD mapping, one combines the switching of two such MLs. There is evidence of noise in the voltage measurement due to the variability of the ON-state resistance, however, the expected trend in switching behavior is seen for all combinations of (W_0, W_1). Taking a $t_{delay} = 5$ ms and performing a statistical t-test, comparing the different switching conditions, there is a statistically significant difference, at the $p = 0.05$level, between the switching of 0, 1, and 2 CRS devices. Additionally, there is no statistical difference between two identical switching conditions, e.g., $(W_0, W_1) = (1, 0)$, $(BL_0, BL_1) = (0, 0)$ and $(W_0, W_1) = (1, 0)$, $(BL_0, BL_1) = (0, 1)$. In other words, we are able to establish unequivocal pattern matching and statistically reliable HD estimation. Therefore, in this paper we demonstrate that it is feasible to use printed CRS arrays as a CAM.

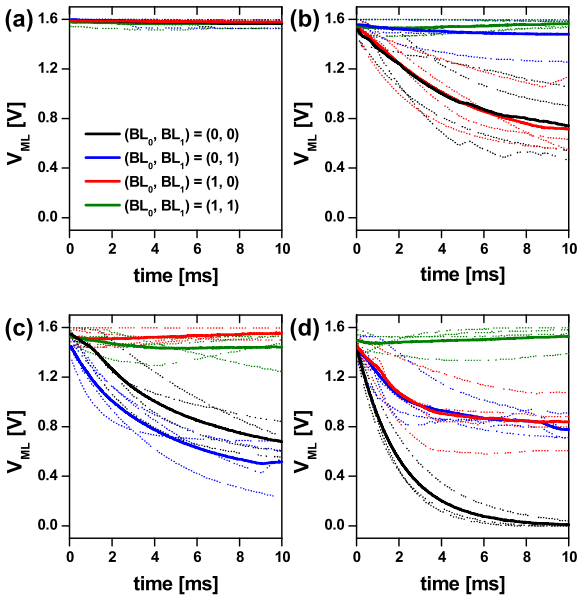

Fig. 6. Single ML voltage $V_{ML}(t)$ measured as a function of time after application of the test pattern to the BLs BL_0 and BL_1 in order to demonstrate HD mapping. Results are shown for (a) $(W_0, W_1) = (0, 0)$, (b) $(W_0, W_1) = (0, 1)$, (c) $(W_0, W_1) = (1, 0)$, and (d) $(W_0, W_1) = (1, 1)$. Four separated 2×2 arrays were tested (dashed lines) and voltages were averaged to determine statistical significance between HD states (bold lines). The read voltage in all cases was 1.6 V and the write voltage was 3 V.

TABLE II
TRUTH TABLE FOR HD MAPPING

Bit lines		Stored data				Hamming distance
BL_0	BL_1	$W_0 = 1$	$W_1 = 0$	$\overline{W_0} = 0$	$\overline{W_1} = 1$	
0	0	ON	-	-	-	1
0	1	ON	-	ON	-	2
1	0	-	-	-	-	0
1	1	-	-	ON	-	1
BL_0	BL_1	$W_0 = 0$	$W_1 = 0$	$\overline{W_0} = 1$	$\overline{W_1} = 1$	Hamming distance
0	0	-	-	ON	ON	2
0	1	-	-	ON	-	1
1	0	-	-	-	ON	1
1	1	-	-	-	-	0

Mapping for the example of storing $(W_0, W_1) = (1, 0)$ and its complement (0, 1), and for storing $(W_0, W_1) = (0, 0)$ and its complement (1, 1) in a 2 x 2 array. ON corresponds to the condition where the CRS device switches and passes through the ON-state window thus leading to a discharge on the ML.

VI. Modeling Larger CRS Arrays

To assess the feasibility of scaling printed CRS arrays to $N \times N$ larger than $N = 2$, we have used a resistor network model that is commonly employed in the literature for RRAM and CRS memory [16], [34], [35]. Model parameters were taken from our experimental measurements and include the ON- and OFF-state resistances and voltage windows, and the resistance of the printed Au lines per unit length ($0.024\ \Omega \cdot \mu\ m^{-1}$). Array sizes up to $N = 128$ were simulated. In our devices, the write disturb window at ~3 V and the read margin for distinguishing the HD states are the most sensitive

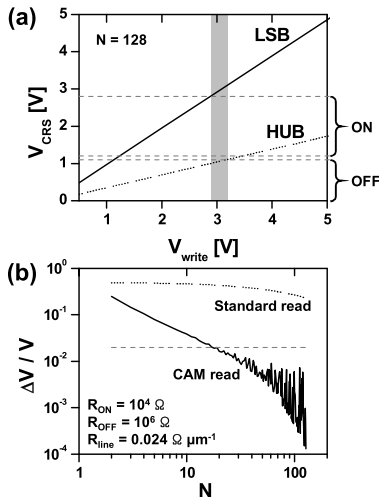

Fig. 7. (a) Write window (gray shaded region) for a 128 × 128 array modeled using the experimental device parameters. LSB = lowest selected bit and HUB = highest unselected bit. Write scheme is a 1/3–2/3 V single-side supply. CRS ON- and OFF-window regions are shown. (b) Read margins $\Delta V/V$ modeled for both a standard one-BL pull-up read and the ML discharge CAM read. A 2% read margin is marked.

parameters to N and are shown in Fig. 7. The read window at ∼1.6 V is degraded if the OFF-state resistance decreases, which would enhance sneak-path current. However, in the CRS devices with $R_{\text{off}} = 10^6\Omega$ we can achieve crosstalk-free operation. At $N = 128$ the width of the write window is only 0.31 V, however, again only disappears completely if the OFF-state resistance is decreased. The main limiting factor is the CAM read, where the difference in ML voltage ΔV_{ML} between ultimate and penultimate HD states must be greater than 2% of the read voltage to avoid noise caused by line resistance. For our system, up to 18 HD states are potentially readable, provided that device-to-device variation is reduced. With future improvements to ON/OFF resistance ratio and smaller feature sizes even larger arrays may be envisaged.

VII. Conclusion

Fully solution-processed CRS device arrays based on the Ag/ZrO_2/Au system are potentially suitable candidates for large-area compatible and printable memory applications. It is possible to operate these devices in small arrays with reasonable cycle endurance and retention times of the memory states. Critically, the switching characteristics allow us to use a conventional 1/3–2/3 V_{write} scheme to program and erase without affecting nonaddressed memory locations, and the complementary structure means that sneak-path currents are eliminated without a separate selector during reading. To improve device-to-device uniformity and memory density, we also scaled the CRS structures down to the limits of our inkjet system, using single ink drops to define each electrode. Finally, we show that we can implement these arrays as CAM by measuring an HD between stored and test data in the array. This is an example of an innovative application, where the integration of printed memory with other large-area electronics could have significant impact on terms of being able to perform basic computation in the vicinity of printed circuits, without having to resort to external or embedded silicon-based devices.

Appendix
Calculation of Wireless Energy Transfer

Wireless data transmission from a large array of sensors over several 10 s of meters becomes unfeasible for an ultralow-power IoT device as illustrated by the following estimation of power requirements for WiFi (802.11g) and Bluetooth LE. Examples of typical energy per bit values for transmit ($E_{\text{b-TX}}$) for these technologies are [36], [37]

$E_{b-\text{TX}}$(Bluetooth LE) = 43 nJ/b

$E_{b-\text{TX}}$(WiFi) = 5.3 nJ/b.

A sensor array of $D \times D$ individual devices operating at f_s gives a data rate $R = D^2 f_s$ and an approximate transmit power $P_{\text{TX}} = E_{b-\text{TX}} R$ assuming continuous broadcasting of data. WiFi is optimized for high R but is not suitable for low-power applications; on the other hand, Bluetooth LE is limited to relatively low R. In terms of power consumption at $f_s = 10$ Hz and $D = 100$, then $P_{\text{TX}} = 4.3$ mW for Bluetooth LE or 0.53 mW for WiFi. Therefore, anything more demanding than this rapidly becomes a problem for an ultralow-power device.

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Jeremy Smith (M'17) received the M.Sci. degree in materials science from the University of Cambridge, Cambridge, U.K., in 2007, and the Ph.D. degree from the Department of Physics, Imperial College London, London, U.K., in 2011.

He is currently a Researcher with the University of California, Berkeley, CA, USA, where he is involved in fully inkjet printable transistors and resistive RAM devices.

Seungjun Chung received the B.S. degree in electrical engineering from Korea University, Seoul, South Korea, in 2006, and the Ph.D. degree in electrical engineering from Seoul National University, Seoul, in 2012.

He joined the Prof. Subramanian's group in electrical engineering, University of California, Berkeley, CA, USA, as a Post-Doctoral Researcher until 2016.He is currently a BK Assistant Professor with the Department of Physics and Astronomy, Seoul National University.

Jaewon Jang (M'17) received the B.S. and master's degrees in electrical engineering from Korea University, Seoul, South Korea, in 2006, and the Ph.D. degree from the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA, USA, in 2013.

He is currently an Assistant Professor with the School of Electronics Engineering, Kyungpook National University, Daegu, South Korea.

Carlos Biaou (M'12) received the B.S. degree in electrical engineering from the University of Maryland, College Park, MD, USA, in 2014. He is currently pursuing the Ph.D. degree in applied sciences and technology with the University of California, Berkeley, CA, USA.

His current research interests include fully printed memory devices for low-cost computation and perovskite solar cells and their degradation processes.

Vivek Subramanian (M'94) received the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, USA, in 1998.

Since 2000, he has been with the University of California, Berkeley, CA, USA, where he is currently a Professor of electrical engineering and computer sciences. His current research interests include printed electronics for display, low-cost logic, and sensing applications.